AMENDMENTS TO THE CLAIMS

1. (Original) A phase adjustment circuit, comprising:

a delay line, the delay line having taps for providing progressively delayed samples of an input signal;

selection circuitry coupled to receive the progressively delayed samples and to receive control signaling to select two samples of the progressively delayed samples; and

an interpolator, consisting essentially of passive elements, coupled to receive the two samples selected and configured to provide a phase-adjusted signal, the phase-adjusted signal being an interpolation of the two samples selected.

2. (Original) The phase adjustment circuit, according to claim 1, further comprising an address select coupled to the selection circuitry, the address select configured to provide the control signaling responsive to an address.

3. (Original) The phase adjustment circuit, according to claim 2, wherein the address select is configured to provide a first select signal and a second select signal for the control signaling.

4. (Original) The phase adjustment circuit, according to claim 3, wherein the first select signal is for selecting a first sample of the two samples, and wherein the second select signal is for selecting a second sample of the two samples.

5. (Original) The phase adjustment circuit, according to claim 4, wherein the first sample and the second sample are associated with two sequentially adjacent taps of the delay line.

6. (Original) The phase adjustment circuit, according to claim 1, wherein the interpolator comprises respective impedances coupled together at a common node for outputting the phase-adjusted signal and wherein an impedance of the respective

impedances is selected from a group consisting of a resistor, an inductor, a capacitor and any combination thereof.

7. (Original) The phase adjustment circuit, according to claim 1, wherein the interpolator comprises sets of impedances coupled in series at respective common output nodes, the common nodes for outputting phase-adjusted signals.

8. (Original) The phase adjustment circuit, according to claim 1, wherein the interpolator comprises:

independent impedances coupled to respective output nodes for providing respective interpolations of the two samples selected; and

a set of impedances coupled to the output nodes and to a common node, the common node for outputting a respective interpolation of the two samples selected.

9. (Original) The phase adjustment circuit, according to claim 8, wherein the respective interpolations and the respective interpolation in combination provide approximately 25, 50 and 75 percent interpolated phases.

10. (Original) The phase adjustment circuit, according to claim 9, wherein the phase-adjusted signal is one of the interpolated phases.

11. (Withdrawn) A phase adjustment circuit, comprising:

a delay line, the delay line having taps for providing progressively delayed samples of an input signal;

interpolators, essentially consisting of passive elements, coupled to receive respective pairs of the progressively delayed samples and configured to provide adjusted phase signals, the adjusted phase signals being respective interpolations of the pairs of the progressively delayed samples; and

selection circuitry coupled to receive the adjusted phase signals and configured to select a phase-adjusted signal of the adjusted phase signals responsive to a control signal.

12. (Withdrawn) The phase adjustment circuit, according to claim 11, further comprising an address select coupled to the selection circuitry.

13. (Withdrawn) The phase adjustment circuit, according to claim 12, wherein the address select is configured to provide the control signal responsive to an address.

14. (Withdrawn) The phase adjustment circuit, according to claim 13, wherein the pairs of the progressively delayed samples are associated with sequentially adjacent taps of the taps.

15. (Withdrawn) The phase adjustment circuit, according to claim 11, wherein each of the interpolators comprises respective impedances coupled in series at a common output node.

16. (Withdrawn) The phase adjustment circuit, according to claim 11, wherein each of the interpolators comprises sets of impedances coupled in series at respective common nodes, the common nodes for outputting the phase-adjusted signals.

17. (Withdrawn) The phase adjustment circuit, according to claim 11, wherein each of the interpolators comprises:

independent impedances coupled to respective output nodes for providing respective interpolations of a respective pair of the pairs of the progressively delayed samples; and

a set of impedances coupled to the output nodes and to a common node, the common node for outputting a respective interpolation of the respective pair.

18. (Withdrawn) The phase adjustment circuit, according to claim 17, wherein the respective interpolations and the respective interpolation in combination provide approximately 25, 50 and 75 percent interpolated phases.

19. (Original) The phase adjustment circuit, according to claim 18, wherein the phase-adjusted signal is one of the interpolated phases.

20. (Original) A method for phase adjustment, comprising:

obtaining an input signal;

generating progressively delayed input signals from the input signal;

using a selector, accessing two of the progressively delayed input signals; and

using only passive elements, interpolating the two of the progressively delayed input signals to provide a phase-adjusted signal.

21. (Original) The method, according to claim 20, wherein the phase-adjusted signal being at least approximately phase aligned with the input signal.

22. (Original) The method, according to claim 21, wherein the accessing comprises:

selecting a progressively delayed input signal of the progressively delayed input signals responsive to an address; and

incrementing the address to select another progressively delayed input signal.

23. (Original) The method, according to claim 22, further comprising:

determining whether phase of the input signal is between the progressively delayed input signal and the other progressively delayed input signal; and

responsive to the phase of the input signal not being between the progressively delayed input signal and the other progressively delayed input signal, adjusting the address to select yet another progressively delayed input signal.

24. (Withdrawn) A method for phase adjustment, comprising:

obtaining an input signal;

generating progressively delayed input signals from the input signal;

accessing pairs of the progressively delayed input signals;

without using phase inversion of the progressively delayed input signals, interpolating the pairs of the progressively delayed input signals to provide phase-adjusted signals; and

selecting a phase-adjusted signal of the phase-adjusted signals as an interpolated output.

25. (Original) An integrated circuit, comprising:

a digital clock module, the digital clock module including:

delay line means having taps for providing progressively delayed samples of an input signal;

selection circuitry means coupled to receive the progressively delayed samples and to receive control signaling to select two samples of the progressively delayed samples; and

interpolator means coupled to receive the two samples selected and configured to provide a phase-adjusted signal, the phase-adjusted signal being an interpolation of the two samples selected.

26. (Original) The integrated circuit, according to claim 25, wherein the selection circuitry means is a multiplexer.

27. (Withdrawn) An integrated circuit, comprising:

a digital clock module, the digital clock module including:

delay line means having taps for providing progressively delayed samples of an input signal;

interpolator means coupled to receive respective pairs of the progressively delayed samples and configured to provide adjusted phase signals, the adjusted phase signals being respective interpolations of the pairs of the progressively delayed samples; and

selection circuitry means coupled to receive the adjusted phase signals and configured to select a phase-adjusted signal of the adjusted phase signals responsive to a control signal.

28. (Withdrawn) The integrated circuit, according to claim 27, wherein the selection circuitry means is a multiplexer.

29. (Original) Phase adjustment circuitry, comprising:

discrete circuits configured to provide respective output signals; and

an interpolator coupled to receive the output signals and configured to provide a phase-adjusted signal, the phase-adjusted signal being an interpolation of the output signals without use of phase inversion of the output signals.

30. (Original) The phase adjustment circuitry, according to claim 29, wherein there are at least two of the output signals.